

claims as attached.

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1. (Three Times Amended) A semiconductor, comprising:

B<sup>1</sup>  
a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the wafer such wafer having a plurality of electrical contacts;

a dielectric member having an electrical conductor thereon, such electrical conductor being elevated above the regions in the fractional portion of the wafer, such electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips, portions of the dielectric member with portions of the electrical conductor thereon spanning the regions in the wafer; and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

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3. The semiconductor recited in claim 2 wherein each one of the voltage generators is disposed in the separating region.

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6. (Amended) A semiconductor, comprising:

B<sup>2</sup>  
a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

an electrical conductor electrically connecting the plurality of electrical selected one or ones of the electrical components to the chips with portions of the electrical conductor elevated above the regions in the fractional portion of the wafer and spanning the separating regions between the chips in the fractional portion of the wafer.

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7. The semiconductor recited in claim 6 wherein each set of electrical components includes a plurality of different electrical components.

B3  
10. (Amended) The semiconductor recited in claim 6 including  
a fusible link electrically connecting a bus disposed in at least one of the plurality of  
integrated circuit chips and a corresponding one of the plurality of electrical components.

11. (Amended) The semiconductor recited in claim 6 wherein each one of the  
electrical components is disposed in the separating region.

12. The semiconductor recited in claim 11 wherein the electrical components are  
voltage generators.

13. (Amended) The semiconductor recited in claim 12 wherein the voltage  
generators are interconnected by the conductor elevated above the regions in the fractional  
portion of the wafer.

14. The semiconductor recited in claim 10 wherein the fusible link is disposed in  
disposed in at least one of the plurality of integrated circuit chips.

15. The semiconductor recited in claim 12 wherein at least one of the voltage  
generators is coupled to more than one bus in corresponding ones of the plurality of  
integrated circuit chips.

B4  
16. (NEW) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated  
circuit chips thereon, such chips being separated by regions in the fractional portion of  
the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

a dielectric member having an electrical conductor thereon, such electrical  
conductor being electrically connected to the plurality of electrical contacts to  
electrically interconnect such plurality of chips, portions of the electrical conductor  
spanning the regions in the fractional portion of the wafer; and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

17. (NEW) The semiconductor package recited in claim 16 wherein each one of the voltage generators is disposed in the separating region.

18. (NEW) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

an electrical conductor electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer, such conductor being elevated above the regions in the fractional portion of the wafer; and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

<sup>9</sup> 20. (NEW) The semiconductor package recited in claim 19 wherein each one of the voltage generators is disposed in the separating region.

<sup>0</sup> 21. (NEW) A semiconductor packaging arrangement, comprising:

(A) a printed circuit board having an electrical interconnect thereon;

(B) a semiconductor package, comprising:

(i) a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the

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B4

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